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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Gerd Frankowsky

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12/27/2005

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EXAMINER

PATEL, PARESH H

ART UNIT

PAPER NUMBER

2829

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/804,582	Applicant(s) FRANKOWSKY ET AL.	
	Examiner Paresh Patel	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 December 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 7-13, 16-20, 23-25 and 27 is/are rejected.
- 7) ☒ Claim(s) 5, 6, 14, 15, 21, 22, 26 and 28 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/15/2005 have been fully considered but they are not persuasive.
2. With respect to claim 1, Applicants' argues that Schnabel does not disclose a switching device to selectively couple the test terminal to the internal voltage line during testing of the first circuit. Examiner disagrees because switching device, which is combination of elements 11, 12 and 8, particularly element 8 (see lines 9-37, column 4) discloses this claimed limitation. Test command evaluation circuit 8 of Schnabel selectively couples (upon application of signal combination which can activate the test circuit 3) the test terminal 5 to the internal voltage line during testing of the first circuit 2.
3. With respect to claim 23, Applicants' argues that Schnabel does not disclose activating a first switch to couple the test terminal to the internal voltage line after application of the activation signal, whereby the internal voltage line is provided with external power for the testing. Examiner disagrees because Schnabel discloses activating (using application of signal combination) a first switch (elements 11, 12 and 8, particularly 8) to couple the test terminal (element 5) to the internal voltage line (voltage line of 2) after application of the activation signal (application of signal combination to activate 3, see lines 9-37 of column 4), whereby the internal voltage line is provided with external power for testing (using 22 and 3).
4. With respect to claims 7-11, 12, 16-19, 23-25 and 27, Applicants' argues that Van Burnt does not teach the limitations as described in a claim(s), at least for three

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reasons (compared with Van Burnt discloser at last paragraph on page 9). After reviewing the Van Burnt as argued, Examiner disagrees because Van Burnt discloses all three reasons, including **a test terminal (21) coupled to the test circuit (40, 20, 22)** in order to provide an activation signal activating the test circuit to perform a test function (for 11) and **a switching device (23)** coupled to an output of the test circuit and configured to **selectively couple** (using 40, via 20, see lines 25-26 of column 4) **the test terminal to the internal voltage line** in response to a switching signal from the output (see lines 9-11 of column 4 and fig. 1).

5. With respect to claims 4, 13 and 20, Applicants' relies on above arguments. Examiner disagrees with Applicants' for the same reason as above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Schnabel (US 6788087).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1 and 23 Schnabel in fig.1-2 discloses an integrated circuit [1], comprising:

- a first circuit [2] to be tested comprising an internal voltage line [voltage line of 2];
- a test circuit [3] for testing the first circuit;
- a test terminal [5] coupled to the test circuit in order to provide an activation signal activating the test circuit to perform a test function [via 8] ; and
- a switching device [11, 12 and 8] to selectively couple the test terminal to the internal voltage line during testing of the first circuit.

Regarding claim 2, Schnabel discloses the test terminal is coupled to the internal voltage line to provide an electrical signal to the internal voltage line from an external source [22].

Regarding claim 3, Schnabel discloses the switching device is further configured to isolate the test terminal from the test circuit after the activation of the test circuit [see Abstract].

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8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 7-11, 12, 16-19, 23-25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Brunt (US 4357703) in view of Tada et al. (US 4801871).

Regarding claims 7, 9, 16 and 23-24, Van Brunt (hereafter Van) discloses a test system [fig. 1] for testing an integrated circuit, comprising:

a first circuit [11] to be tested comprising an internal voltage line;

a test circuit [40, 20, 22] for testing the first circuit;

a test terminal [21] coupled to the test circuit in order to provide an activation signal activating the test circuit to perform a test function [test data input];

a switching device [23] coupled to an output of the test circuit and configured to selectively couple [using 40] the test terminal to the internal voltage line [of 11] in response to a switching signal from the output.

Van discloses all the elements including an external test device [lines 1-3 of column 4] connected to the integrated circuit via the test terminal. Van is silent about said external test device comprising (i) a test module for issuing the activation signal; and (ii) a power supply for providing an electrical signal to the internal voltage line after the activation of the test circuit.

Tada et al. (hereafter Tada) in fig. 1 and 4 discloses the external test device [30] comprising (i) a test module [D and C] for issuing the activation signal; and (ii) a power

supply [PS, GND] for providing an electrical signal to the internal voltage line after the activation of the test circuit [1].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to replace tester of Van with tester as taught by Tada, in order to test circuits without changing wiring boards and to reduce testing cost.

Regarding claim 17, Tada discloses (in fig. 4) the external test device further comprises an external test device switch [programmable R1, R2, RV and RG] for selectively coupling the test module and power supply to the test terminal.

Regarding claims 8, 18 and 25, Van discloses the test circuit is configured to output the switching signal in response to receiving the activation signal.

Regarding claims 10, 19 and 27, Van discloses the switching device is further configured to isolate the test terminal from the test circuit after the activation of the test circuit.

Regarding claim 12, Van discloses the test circuit is configured to deactivate as claimed.

Regarding Claim 11, the combination of Van and Tada discloses all the elements except for test circuit comprise a memory element to store activation information. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use memory element as claimed for storing the information, since it was known in the art to store the information for programming including control application.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schnabel as applied to claim 1 above, and further in view of Horiguchi et al. (US 5347492).

Regarding claim 4, Schnabel discloses all the elements except for the first circuit further comprise an internal voltage supply. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use internal voltage supply to operate partial circuit, since it was known in the art to reduce the power consumption of the integrated circuit [see lines 15-21 of column 1, US 5347492].

11. Claims 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van and Tada as applied to claims 7 and 16 above, and further in view of Horiguchi et al. (US 5347492).

Regarding claims 13 and 20, the combination of Van and Tada discloses all the elements except for the first circuit further comprise an internal voltage supply. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use internal voltage supply to operate partial circuit, since it was known in the art to reduce the power consumption of the integrated circuit [see lines 15-21 of column 1, US 5347492].

Allowable Subject Matter

12. Claims 5-6, 14-15, 21-22, 26 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. See office action dated 09/15/2005 for reason for allowance.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

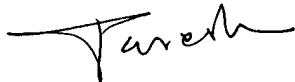
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 571-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



December 21, 2005

Paresh Patel
Primary Examiner
Art Unit 2829